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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,784	09/24/2003	James.C. Farmer	10002762-3	6401

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,784	FARMER ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Remarks filed on April 3, 2007 regarding application 10,669,784 filed on September 24, 2003.

2. Claims 2 and 17 have been cancelled.

Claims 1, 3-16 and 18-20 are pending under consideration.

3. ***Response to Remarks and Amendments***

Applicants' amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Applicants contended that "key data" as recited in claim 1 means "data employed to establish authorization to store the data in the pertinent storage device," and Garcia's CRC bits do not qualify as "key data." The Examiner disagrees.

First, Garcia teaches that memory protection is provided by an access validation method maintained by each CPU in which CPUs and/or I/O devices are provided with a validation to read/write memory of that CPU, without which memory access is denied (abstract).

Second, Garcia further teaches "access validation" in details from column 30, lines 56 through column 37, lines15.

Third, Garcia specifically teaches that "Accesses to the memory 28 are validated by the AVT logic 90 of each interface unit 24 (FIG. 5), using all of six checks: (1) that the CRC of the message packet carrying the request is error free, ..." (column 31, lines 10-25).

Thus, Garcia clearly teaches using the CRC bits to establish authorization to access memory. As such, the Examiner's position regarding the patentability of all claims remains the same as stated in the previous Office Action.

4. ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Garcia et al. (US 6,151,689).

It is noted that, in the following claim analysis, those elements recited by the claims are presented using **bold** font.

As to claim 1, Garcia et al. discloses **a method for protecting memory space in a target storage device during a write operation in a computer system** [CPUs and I/O devices may write to, or read from, memory of a CPU of the system. Memory protection is provided by an access validation method maintained by each CPU in which CPUs and/or I/O devices are provided with a validation to read/write memory of that CPU, without which memory access is denied (abstract)], **the method comprising**:

creating a single data packet [figures 3A~3D and 4A~4C show various types of packets, comprising Header, Address, data and CRC], **including user data** [figures 3A~3D and 4A~4C show various types of packets, comprising Header, Address, data and CRC] **that is to be written to said target storage device** [figure 6, 24b is the target storage device] **and key data** [for example, the CRC may be the corresponding key data; Accesses to the memory 28 are validated by the AVT logic 90 of each interface unit 24 (FIG. 5), using all of six checks: (1) that the CRC of the message packet carrying the request is error free, ..." (column 31, lines 10-25)] **that is used to establish authorization to store said user data** [Use of CRC in this manner operates to protect message packets from end to end because the router elements do not modify or regenerate the CRC as the message packet passes through. The CRC of each message packet is checked at each router crossing. A command symbol--"This packet Good" (TPG) or "This Packet Bad" (TPB)--is appended to every packet (column 5, lines 39-45); Garcia further teaches "access validation" in details from column 30, lines 56 through column 37, lines15];

transmitting said single data packet to the target storage device [see figure 6];

determining whether said key data is valid [If the received message packet is found to have a bad CRC (or it is tagged with a "This Packet Bad" (TPB) command symbol, see below) the packet is discarded, and access is denied (column 31, lines 22-25)];

writing said user data into said target storage device only when said key data is valid [CPUs and I/O devices may write to, or read from, memory of a CPU of the system. Memory protection is provided by an access validation method maintained by

each CPU in which CPUs and/or I/O devices are provided with a validation to read/write memory of that CPU, without which memory access is denied (abstract)].

As to claim 3, Garcia et al. teaches that **the method of claim 1 further comprising:**

performing a Boolean operation on selected bits of said user data to generate said key data [for example, the CRC may be the corresponding key data, which is calculated based on Boolean operations on Data bits].

As to claim 4, Garcia et al. teaches that **the method of claim 1 further comprising**:

generating verification data from said user data at a controller of said target storage device [Error-checking of the communication flow between the components of the processing system is achieved by adding a cyclic-redundancy-check (CRC) to the message packets that are sent between the elements of the system (column 5, lines 28-31)]; **and**

comparing said key data in said single data packet with said verification data to determine if said key data matches said verification data [The CRC of each message packet is checked not only at the destination of the message, but also while en route to the destination by each router element used to route the message packet from its source to the destination. If a message packet is found by a router element to have an incorrect CRC, the message packet is tagged as such, and reported to a maintenance diagnostic system (column 5, lines 31-40)].

As to claim 5, Garcia et al. teaches that **the method of claim 4 further comprising: storing said user data to said target storage device if said key data matches said verification data** [CPUs and I/O devices may write to, or read from, memory of a CPU of the system. Memory protection is provided by an access validation method maintained by each CPU in which CPUs and/or I/O devices are provided with a validation to read/write memory of that CPU, without which memory access is denied (abstract)].

As to claim 6, Garcia et al. teaches that **the method of claim 1 further comprising:**

generating key data based on a destination address of said write operation [Accesses to the memory 28 are validated by 2) that the destination (e.g., CPU 12A) identified in the message packet is that of the receiver (column 31, lines 13-15)].

As to claim 7, Garcia et al. teaches that **the method of claim 1 further comprising:**

generating key data based on a system clock setting of said computer system [FIG. 7B is an block diagram of a construction of the clock synchronization FIFO structure shown in FIG. 7A].

As to claim 8, refer to "As to claim 1."

As to claim 9, refer to "As to claim 5."

As to claim 10, refer to "As to claim 2."

As to claim 11, refer to "As to claim 2."

As to claim 12, refer to "As to claim 4."

As to claim 13, refer to "As to claim 5."

As to claim 14, refer to "As to claim 7."

As to claim 15, refer to "As to claim 1."

As to claim 16, refer to "As to claim 5."

As to claim 18, refer to "As to claim 3."

As to claim 19, refer to "As to claim 4."

As to claim 20, refer to "As to claim 4." Also see figure 6 of Garcia et al.

Conclusion

6. Claims 1, 3-16 and 18-20 are rejected as explained above.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

May 4, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
5/a/07